REMARKS

Claims 1-13 are pending in the application.

By way of this response, Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that the examiner telephone Peter Scott at (719)533-7969 so that such issues may be resolved as expeditiously as possible.

Response to the rejection under 35 U.S.C. § 103

Claims 1, 2, 7, 8, 12, 13 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Si et al., U.S. Patent No. 4,819,166 (*Si*) in view of Cliff et al., U.S. Patent No. 6,023,439 (*Cliff*) and Agrawal, U.S. Patent No. 6,341,092 B1 (*Agrawal*). Applicant respectfully traverses the rejection as follows.

Regarding Claim 1, the rejection alleges in section 3 that *Si* discloses the claimed latch based random access memory except for the claimed input data register, the claimed input data buffer coupled to the input data register, the claimed latch array coupled to the input data buffer, and the claimed latch array bypass multiplexer. In other words, the rejection admits that *Si* does not disclose any of the claimed elements in the claimed relationship to one another.

The rejection further proposes to modify *Si* to include the RAM block (447) and the column decoder (448) of FIG. 21B in *Cliff*. However, the rejection fails to establish the alleged equivalence between the RAM block (447) and the column decoder (448) in *Cliff* and the input data register and the input buffer recited in Claim 1. If the rejection is not

withdrawn, Applicant requests that the alleged equivalence between the the RAM block (447) and the column decoder (448) in *Cliff* and the claimed elements be clearly explained. Further, the rejection fails to provide a reasonable explanation of how the proposed modification to *Si* by *Cliff* might be made, that is, specifically how the RAM block (447) and the column decoder (448) would be connected in FIGS 2 and 6 of *Si* as proposed by the rejection. Absent such an explanation, the proposed modification lacks sufficient support to sustain the rejection of Claim 1 under 35 U.S.C. § 103.

The rejection then proposes to modify the combination of *Si* and *Cliff* by *Agrawal* to arrive at the claimed invention. The rejection alleges that *Agrawal* discloses the claimed latch array bypass multiplexer in FIG. 3 and column 7, lines 5-24. However, *Agrawal* does not show in FIG. 3 nor does *Agrawal* disclose in column 7, lines 5-24 that the multiplexers (132, 134, 136) bypass the latches (120, 122,124). Because *Agrawal* does not disclose multiplexers that bypass the latches, the modification proposed by the rejection fails to arrive at the claimed invention. The rejection further fails to provide a reasonable explanation of how the proposed modification might be made, that is, how the multiplexers in *Agrawal* would be connected to the combination of *Si* and *Cliff* to arrive at the claimed invention. Absent such an explanation, the proposed modification lacks sufficient support to sustain the rejection of Claim 1 under 35 U.S.C. § 103.

Regarding Claim 2, the rejection alleges that *Si*, *Cliff*, and *Agrawal* teach the additional limitations of the claimed read address register and the claimed read address multiplexer coupled to the read address register for selecting

one of a logic scan address and a memory scan address in response to the memory scan mode signal. However, the rejection cites only FIG. 5 and column 8, lines 4-11 in *Agrawal*, which may reasonably be construed as an admission by the PTO that neither *Si* nor *Cliff* teach the limitations of Claim 2. Further, *Agrawal* does not show the claimed read address multiplexer coupled to the read address register for selecting one of a logic scan address and a memory scan address in response to the memory scan mode signal in FIG. 5. Also, the reference to multiplexers in column 8, lines 4-11 in *Agrawal* does not teach or suggest that the multiplexers are coupled to the read address register for selecting one of a logic scan address and a memory scan address in response to the memory scan mode signal as alleged by the rejection. Because neither *Si*, *Cliff*, or *Agrawal* teach or suggest the claimed read address register and the claimed read address multiplexer coupled to the read address register for selecting one of a logic scan address and a memory scan address in response to the memory scan mode signal, the proposed modification lacks sufficient support to sustain a rejection of Claim 2 under 35 U.S.C. § 103.

Further, even if *Agrawal* did teach or suggest the claimed read address register and the claimed read address multiplexer coupled to the read address register for selecting one of a logic scan address and a memory scan address in response to the memory scan mode signal, the rejection fails to provide a reasonable explanation of how the proposed modification might be made, that is, how the elements in *Agrawal* would be connected to the combination of *Si* and *Cliff* to arrive at the claimed invention. Absent such an explanation, the proposed modification lacks sufficient support to sustain the rejection of Claim 2 under 35 U.S.C. §

103.

Regarding Claim 7, the rejection alleges that *Si*, *Cliff*, and *Agrawal* teach the additional limitations of:

(a) modifying a latch based memory to include a latch array bypass multiplexer for selecting one of an input data buffer of the latch based random access memory and a latch array of the latch based random access memory for generating a first data output of the latch based random access memory from the input data buffer during logic scan testing and a second data output of the latch based random access memory from the latch array during memory scan testing in response to a memory scan mode signal;

(b) asserting the memory scan mode signal during a memory scan test; and

(c) removing the memory scan mode signal during a logic scan test.

However, the rejection fails to show that Cliff teaches the claimed input data register and the claimed input buffer as explained above. Further, the rejection fails to show that *Agrawal* teaches or suggests modifying a latch based memory to include a latch array bypass multiplexer for selecting one of an input data buffer of the latch based random access memory and a latch array.

Regarding Claim 8, the rejection alleges that *Si*, *Cliff*, and *Agrawal* teach the additional limitation of selecting one of a logic scan address and a memory scan address for coupling to a read address register of the latch based random access memory in response to the memory scan mode signal. However, the rejection cites only FIG. 5 and column 8, lines 4-11 in *Agrawal*, which may reasonably be construed as an admission by the PTO that neither *Si* nor *Cliff* teach the limitations of Claim 8. Further, *Agrawal* does not show the

claimed read address multiplexer coupled to the read address register for selecting one of a logic scan address and a memory scan address in response to the memory scan mode signal in FIG. 5. Also, the reference to multiplexers in column 8, lines 4-11 in *Agrawal* does not teach or suggest that the multiplexers are coupled to the read address register for selecting one of a logic scan address and a memory scan address in response to the memory scan mode signal as alleged by the rejection. Because neither *Si*, *Cliff*, or *Agrawal* teach or suggest the claimed read address register and the claimed read address multiplexer coupled to the read address register for selecting one of a logic scan address and a memory scan address in response to the memory scan mode signal, the proposed modification lacks sufficient support to sustain a rejection of Claim 2 under 35 U.S.C. § 103.

Regarding Claim 12, the rejection alleges that *Si*, *Cliff*, and *Agrawal* teach the additional limitation of bypassing logic chains surrounding the latch based random access memory during a memory scan test. However, the rejection cites only FIG. 3 and column 7, lines 5-24 in *Agrawal*, which may reasonably be construed as an admission by the PTO that neither *Si* nor *Cliff* teach the limitations of Claim 12. Further, *Agrawal* does not show bypassing logic chains in FIG. 3, nor does *Agrawal* teach or suggest bypassing logic chains in column 7, lines 5-24 as alleged by the rejection.

Regarding Claim 13, the rejection alleges that *Si*, *Cliff*, and *Agrawal* teach the additional limitation of bypassing the latch array during a logic scan test. However, the rejection cites only FIG. 3 and column 7, lines 5-24 in *Agrawal*, which may reasonably be construed as an admission by the PTO that neither *Si* nor *Cliff* teach the limitations of

Claim 13. Further, *Agrawal* does not show bypassing logic chains in FIG. 3, nor does *Agrawal* teach or suggest bypassing the latch array in column 7, lines 5-24 as alleged by the rejection.

Claims 4 and 10 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over *Si*, *Cliff*, *Agrawal*, Lach, et al., U.S. Patent No. 5,909,451 (*Lach*), and further in view of Sindhu, U.S. Patent No. 5,123,101 (*Sindhu*). Applicant respectfully traverses the rejection as follows.

Regarding Claims 4 and 10, the rejection alleges in section 5 that *Sindhu* discloses the claimed bypass logic for controlling the latch array bypass multiplexer in response to the memory scan mode signal and the scan mode signal in FIG. 4 and column 12, lines 34-35. However, as may easily be seen in *Sindhu*'s FIG. 4, the bypass multiplexer (138) does not function in a latch based random access memory. Consequently, the bypass multiplexer (138) would not work in the proposed modification to arrive at the claimed invention as alleged by the rejection, even if the rejection provided a reasonable explanation of how the proposed modification might be made from five disparate devices. Because the bypass multiplexer (138) would not work in the proposed modification to arrive at the claimed invention, and because the rejection fails to provide a reasonable explanation of how the proposed modification might be made, the proposed modification lacks sufficient support to sustain a rejection of Claim 2 under 35 U.S.C. § 103.

No additional fee is believed due for this amendment.

Respectfully submitted,

/ Eric James Whitesell /

Eric James Whitesell

Reg. No. 38,657

Address all correspondence to:

LSI Logic Corporation

1621 Barber Lane, M/S D-106

Milpitas, CA 95035-7458

Direct telephone inquiries to:

Peter Scott

(719) 533-7969